AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1 – 14 (cancelled).

15. *(withdrawn)* A method for manufacturing a multi-level circuit substrate, comprising:

a step of forming a lower interconnect layer on an underside of a lower insulation layer, and a lower connection member inside of and penetrating through the lower insulation layer in a thickness direction thereof and electrically connected with the lower interconnect layer;

a step of forming an intermediate connection layer electrically connected with the lower interconnect layer on an upper surface of the lower insulation layer, and a shield layer placed spaced from around the intermediate connection layer;

a step of forming a coat layer on the upper surface of the lower insulation layer, and forming in the coat layer an opening substantially coincident with a gap between the intermediate connection layer and the lower interconnect layer;

a step of forming an insulator lower in specific dielectric constant than the lower insulation layer, and removing the insulator together with the coat layer except for the insulator on the opening;

a step of forming an upper insulation layer equivalent in specific dielectric constant to the lower insulation layer on the upper surface of the lower insulation layer;

a step of forming an upper connection member inside of and penetrating through the lower insulation layer in a thickness direction thereof and electrically connected with the intermediate connection layer; and

a step of forming an upper interconnect layer electrically connected with the upper connection member on an upper surface of the upper insulation layer.

16. *(new)* A multi-level circuit substrate comprising:

upper and lower parallel non-aligned interconnect layers respectively extending inwardly horizontally from opposite sides of the substrate and having an end termination at a central location in the substrate;

insulation provided between the two interconnect layers;

at least two vertically aligned conductors each respectively extending perpendicularly from one of the interconnect layers through the insulation and each having an inner end centrally of the substrate;

an intermediate connection layer in a horizontal plane sandwiched between and in contact with the inner ends of the aligned conductors so as to provide an electrical connection between the upper and lower non-aligned interconnect layers;

a shield layer provided in approximately the same horizontal plane as the intermediate connection layer and surroundingly spaced from and around the intermediate connection layer; and

wherein a condition of $(R \bullet r) / (2 \bullet h) \leq L \leq (5 \bullet R \bullet r) / h$ is satisfied, provided that a connection distance between the interconnect layers through the aligned conductors and the intermediate connection layer is h, the aligned conductors are circular cylinders having a diameter R, the intermediate connection layer has a circular periphery portion having a diameter r, and a spaced distance between the intermediate connection layer and the shield layer is L.

17. *(new)* A multi-level circuit substrate according to claim 16, wherein the insulation comprises stacked layers including a lower or first insulation layer, a second insulation layer stacked on top of the lower insulation layer, a third insulation layer stacked on the second insulation layer and a fourth or top insulation layer stacked on the third insulation layer and, wherein the shield layer is sandwiched between the second insulation layer and the third insulation layer; and

wherein the aligned conductors comprise a lower conductor electrically connecting the lower interconnect layer and the intermediate connection layer and an upper conductor electrically connecting the intermediate connection layer to the upper interconnect layer.

18. *(new)* A multi-level circuit substrate according to claim 16, wherein the shield layer is a ground layer.

19. *(new)* A multi-level circuit substrate according to claim 16, wherein the shield layer is a power source layer.

20. *(new)* A multi-level circuit substrate according to claim 16, wherein the multi-level circuit substrate transmits a signal having a wavelength shorter than 1500 times the connection distance h.

21. *(new)* A multi-level circuit substrate comprising:

upper and lower interconnect layers vertically spaced relative to each other;

a first insulator provided between the upper and lower interconnect layers;

upper and lower conductors provided in the insulation material between the interconnect layers with the upper connection member contacting the upper interconnect layer and the lower connection member contacting the lower interconnect layer;

an intermediate connection layer sandwiched between and contacting the upper and lower conductors so as to complete an electrical connection between the interconnect layers;

a shield layer provided in alignment with and surrounding the intermediate connection layer and placed while being spaced from the intermediate connection layer by a gap; and

a second insulator having a lower specific dielectric constant than the first insulator positioned in the gap between the shield layer and the intermediate connection layer.

22. *(new)* A multi-level circuit substrate according to claim 21, wherein a condition of $(R \bullet r \bullet \sqrt{\varepsilon'}) / (2 \bullet h \bullet \sqrt{\varepsilon}) \leq L \leq (5 \bullet R \bullet r \bullet \sqrt{\varepsilon'}) / (h \bullet \sqrt{\varepsilon})$ is satisfied, provided that the specific dielectric constant of the first insulator is ε, the specific dielectric constant of the second insulator is ε', the connection distance between the interconnect layers through the connection members and the intermediate connection layer is h, the upper and lower conductors are generally formed as a circular cylinder having a diameter R, the intermediate connection layer is generally circular having a diameter r, and the spaced distance between the intermediate connection layer and the shield layer is L.

23. *(new)* A multi-level circuit substrate according to claim 21, wherein the first insulator is formed of lower and upper stacked upper and lower insulation layers;

the intermediate connection layer and the shield layer are sandwiched between the lower insulation layer and the upper insulation layer; and

wherein the connection members comprise a lower connection member provided in the lower insulation layer and electrically connecting the lower interconnect layer and the intermediate connection layer; and

an upper connection member provided in the upper insulation layer and electrically connecting the upper interconnect layer and the intermediate connection layer.

24. *(new)* A multi-level circuit substrate according to claim 21, wherein the shield layer is a ground layer.

25. *(new)* A multi-level circuit substrate according to claim 21, wherein the shield layer is a power source layer.

26. *(new)* A multi-level circuit substrate according to claim 21, wherein the multi-level circuit substrate transmits a signal having a wavelength shorter than 1500 times the connection distance between the interconnect layers through the upper and lower conductors and the intermediate connection layer.

27. *(new)* A multi-level substrate as recited in claim 16, wherein the intermediate connection layer has a circular peripheral surface.

28. *(new)* A multi-level substrate as recited in claim 27, wherein the end termination of the upper interconnect layer and the lower interconnect layer each include a connection land that is generally circular in plan and positioned to contact a respective one of the aligned conductors and an outwardly extending arm having parallel edges.

29. *(new)* A multi-layer substrate as recited in claim 27, wherein the shield layer has a circular cut-out defined by a circular surface spaced from and surrounding the intermediate connection layer.

30. *(new)* A multi-level circuit substrate comprising:

mutually opposing connection lands provided inward of the substrate;

at least a pair of non-aligned interconnect layers comprising upper and lower interconnect layers provided inward of the substrate and being respectively connected to the connection lands;

insulators provided between the upper and lower interconnect layers;

at least two substantially cylindrical connection members aligned on a line that passes through the insulators and are each respectively electrically connected with a respective one of the connection lands;

a substantially circular intermediate connection layer oriented in a plane sandwiched between the connection members to electrically connect the connection members;

a shield layer provided in approximately the same plane as the intermediate connection layer and surroundingly spaced from and around the intermediate connection layer; and

wherein a condition of $(R \bullet r) / (2 \bullet h) \leq L \leq (5 \bullet R \bullet r)/h$ is satisfied, provided that a connection distance between the interconnect layers through the interconnect layers and the intermediate connection layer is h, a diameter of the substantially cylindrical connection members is R, a diameter of the substantially circular intermediate connection layer is r, and a spaced distance between the intermediate connection layer and the shield layer is L.

31. *(new)* A multi-level circuit substrate according to claim 30, wherein the insulation comprises stacked layers including a lower or first insulation layer, a second insulation layer stacked on top of the lower insulation layer, a third insulation layer stacked on the second insulation layer and a fourth or top insulation layer stacked on the third insulation layer and, wherein the shield layer is sandwiched between the second insulation layer and the third insulation layer; and

wherein the aligned conductors comprise a lower conductor electrically connecting the lower interconnect layer and the intermediate connection layer and an upper conductor electrically connecting the intermediate connection layer to the upper interconnect layer.

32. *(new)* A multi-level circuit substrate according to claim 30, wherein the shield layer is a ground layer.

33. *(new)* A multi-level circuit substrate according to claim 30, wherein the shield layer is a power source layer.

34. *(new)* A multi-level circuit substrate according to claim 30, wherein the multi-level circuit substrate transmits a signal having a wavelength shorter than 1500 times the connection distance h.